

I/O CIRCUIT USING LOW VOLTAGE TRANSISTORS WHICH CAN
TOLERATE HIGH VOLTAGES EVEN WHEN POWER SUPPLIES ARE
POWERED OFF

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CROSS-REFERENCE TO RELATED APPLICATIONS

- 4/19/04
- [0001] This application is a continuation-in-part of Application No. 10/043,788, filed January 9, 2002, ^{Now US P 6,628,149} which claims the benefit of U.S. Provisional Application No. 60/260,580, filed January 9, 2001, and U.S. Provisional Application No. 60/260,582, filed January 9, 2001, all three of which are hereby incorporated by reference in their entirety; and this application also claims the benefit of U.S. Provisional Application No. 60/427,954, filed November 21, 2002, which is hereby incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

- [0002] The present invention relates to integrated circuits (ICs), such as interface circuits, that are designed having reduced feature sizes, for example, 0.13 μm . More particularly, the invention relates to ICs that include interfaces (such as input/output (I/O) circuits) that are capable of interfacing with comparatively high-voltage signals from other sources, for example a 3.3 volt IC interfacing with signals from a 5 volt IC, or any other disparate ranges. Moreover, the invention relates to integrated circuits in which the semiconductor devices are biased such that the stress across the gate-oxides and junctions, as well as the leakage currents, are maintained at tolerable levels.